I claim:

1. An integrated circuit comprising:

A. core circuitry including functional inputs and functional outputs;

B. an input pad;

C. scan distributor circuitry connected between the input pad and, selectively, at least some of the functional inputs;

D. an output pad; and

E. scan collector circuitry connected selectively between at least some of the functional outputs and the output pad.

2. The integrated circuit of claim 1 including controller circuitry connected to the scan distributor circuitry, the scan collector circuitry and the core circuitry.

3. The integrated circuit of claim 1 including multiplexer circuitry selectively connecting the scan distributor circuitry to at least some of the functional inputs.

4. The integrated circuit of claim 1 including demultiplexer circuitry selectively connecting at least some of the functional outputs to the scan collector circuits.

5. The integrated circuit of claim 1 including plural core circuits, each with its own scan distributor and collector circuits selectively connected to at least some of the respective functional inputs and outputs.

6. The integrated circuit of claim 1 including plural core circuits, each with its own scan distributor and collector circuits selectively connected to at least some of the respective functional inputs and outputs, the scan distributor and collector circuits of one core circuitry being connected in a hierarchy with the scan distributor and collector circuits of another core circuit.

7. Integrated circuit core circuitry comprising:

A. functional circuitry having plural functional inputs and plural functional outputs and including parallel scan paths;

B. scan distributor circuitry having a serial input connected to a functional input and a serial output connected to a functional output and having parallel outputs connected to inputs of the parallel scan paths; and

C. scan collector circuitry having a serial input connected to a functional input and a serial output connected to a functional output and parallel inputs connected to outputs of the parallel scan paths.

8. An integrated circuit including plural core circuitry of claim 7 including functional outputs of one core circuitry being connected to functional inputs of another core circuitry and functional outputs of the another core circuitry connected to the functional inputs of the one core circuitry to connect the serial output of one scan distributor to the serial input of another scan distributor and to connect the serial output of one scan collector to the input of another scan collector.

9. The integrated circuit of claim 8 including multiplexer and demultiplexer circuitry selectively connecting the functional outputs to the functional inputs.

10. The integrated circuit of claim 8 in which the serial output of the one scan distributor connects through one functional output and functional inputs of plural cores

to the serial input of plural scan distributors.

11. The integrated circuit of claim 8 in which the serial output of plural scan distributors connects through plural functional outputs and one functional input to the serial input of the one scan distributor.

12. The integrated circuit of claim 8 in which the serial input of the one scan collector connects through one functional input of the one core and plural functional outputs of plural cores to the serial output of plural scan collectors.

13. The integrated circuit of claim 8 in which the serial output of the one scan collector connects through one functional output and plural functional inputs to the serial input of plural scan collectors.

14. A process of transferring information comprising;

A. transferring functional data from a pad on an integrated circuit to first core circuitry on the integrated circuit;

B. transferring functional data from the first core circuitry to the pad on the integrated circuit;

C. transferring functional data from the first core circuitry to second core circuitry on the integrated circuitry;

D. transferring functional data from the second core circuitry to the first core circuitry;

E. transferring test data from the pad to the second core circuitry via the first core circuitry.

15. The process of claim 14 in which the first core circuitry is one of a digital signal processor, microcontroller, and microprocessor.

16. The process of claim 14 in which the second core circuitry is one of a random access memory, analog to digital converter, digital to analog converter, and I/O peripheral.

17. An integrated circuit comprising;

a data input pad;

a first core circuit having a data input terminal and data output terminal;

a second core circuit having a data input terminal;

a first connection formed between the data input pad and the data input terminal of the first core circuit;

a second connection formed between the data output terminal of the first core circuit and the data input terminal of the second core circuit; and

a scan distributor between the data input and output terminals of the first core circuit.

18. The integrated circuit of claim 17 wherein the first core circuit is one of a digital signal processor, microcontroller, and microprocessor.

19. The integrated circuit of claim 17 wherein the second core circuit has a data output terminal and the second core circuit includes a scan distributor between the data input and output terminals of the second core circuit.

20. An integrated circuit comprising;

a data output pad;

a first core circuit having a data output terminal and data input terminal;

a second core circuit having a data output terminal;

a first connection formed between the data output pad and the data output terminal of the first core circuit;

a second connection formed between the data input terminal of the first core circuit and the data output terminal of the second core circuit; and

a scan collector between the data input and output terminals of the first core circuit.

21. The integrated circuit of claim 20 wherein the first core circuit is one of a digital signal processor, microcontroller, and microprocessor.

22. The integrated circuit of claim 20 wherein the second core has a data input terminal and a scan collector exists between the data input and output terminals of the second core circuit.

23. A process of manufacturing an integrated circuit comprising;

forming a core circuit on an integrated circuit to have a functional parallel data input bus and a functional parallel data output bus;

forming at least one test data input on the functional parallel data input bus; and

forming at least one test data output on the functional parallel data output bus.